Jerry E. McGoveran

Certus Consulting Group, Inc.

IC Design and Verification

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AREAS OF EXPERTISE

All aspects of high-speed, high-density ASIC and System on Chip (SoC) development and test, including specification, vendor selection, project management, design, logic synthesis, verification, timing closure, clock tree synthesis, circuit analysis, cell design, floorplanning, physical design, design for test (DFT), test development, and failure analysis.

CONSULTING EXPERIENCE – 1989 to present

SanDisk, Milpitas, CA

- Hardware/Firmware co-verification of Flash Controller SoCs. Verification and failure debug of firmware, RTL and gate level designs. Test development, code coverage, regression testing, Perl and shell scripting, C debug. AHB bus model design.

Microsoft, Mt. View, CA

- Design verification of 100M gate Graphics Processing Unit SoC. Debug of RTL and gate level simulations. Revision control, simulation environment setup, regression testing, code coverage, data reduction, Perl and shell scripting, C/C++ debug.

Sigma Design/Blue7 Communications, Milpitas, CA

- Design local bus interface and DMA packet transfer logic from specification. Verilog RTL coding and simulation.

Texas Instruments, San Jose, CA

- RTL design of DFT logic in Voice Over IP SoC. Defined, designed and integrated test mode control for scan, burnin, PLL, PCM, IODFT, IDDQ, memory BIST, JTAG, ICE, and multiple tester modes.
- Top-level verification lead -10M gate Broadband SoC containing 3 DSP cores and an ARM7 uP core. Managed team of verification engineers writing DSP ROM assembly code to exercise DSPs and peripherals, DMA transfers among DSPs, the ARM7 and peripherals, and core logic. Wrote bus functional model for ARM management port I/F used for ROM code debug.
- Specialized support for problem ASIC designs, typically large networking chips. Optimize speed, density and performance. Identify roadblocks to successful tapeout and work closely with my client's customers to develop and implement solutions. Logic synthesis, timing closure, floorplanning, physical design, clock tree optimization, test program and prototype debug, project management, scan chains, JTAG, ATPG, optimize test time and coverage. Supervise junior engineers in delegated tasks.
- Re-design and analysis of legacy high-speed, Data Buffer Chip used with UltraSparc processor and SRAM with 500MHz system clock speed. Extensive SPICE analysis and timing tweaks of IO timing paths. Design custom buffer cells for clock trees. Optimize on-chip PLL loopback delays to sync with board level system and minimize jitter and skew. Extensive backend physical design, manual layout of clock trees and PLL loops to correct signal integrity issues. Wrote and modified C programs to adjust legacy test vectors for reuse with higher clocking rates and clock ratios.

Chameleon Systems, San Jose, CA

- DFT and ATPG for 2M gate configurable uP chip. Modify/rewrite existing scripts from earlier design to improve test coverage and reduce vector count using Mentor Graphics DFTAdvisor and Fastscan.

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CONSULTING EXPERIENCE (cont.)

Cellnet Data Systems, San Carlos, CA
- Top-level verification lead for SoC Utility Meter Reader/Transmitter. Testbench development, logic verification, test vector generation, DFT, fault coverage analysis, and ASIC development support.

Sun Microsystems, Inc., Mt. View, CA
- Verification, timing analysis, for a six-chip UltraSPARC processor system chipset. Updated Verilog design database to more recent software release to allow IP encryption. Document comprehensive timing spec for release to chipset design-in customers and technology partners.

Vadem, San Jose, CA
- Independent design review and risk analysis of 60K gate ASIC prior to prototyping. Wrote C code utilities to analyze netlist and wire delay files for potential performance problems.
- Fault simulator product evaluation. Wrote fault simulation training manual.

Quantum Corp., Milpitas, CA
- Design and verification for 12 different chip projects including SCSI I/F controllers, integrated Disk/IDE or Disk/SCSI controllers, some with embedded uP. Responsible for RTL design and logic synthesis, RTL and gate level simulation, timing closure, testbench development, test generation, DFT, floorplanning and physical design, vendor evaluation, fault simulation, writing C and shell script utilities. Lab work for failure analysis and prototype bringup. Transistor level design of SCSI IO cell.

Systron Donner Inertial, Concord, CA
- Frontend and backend design for Inertial Guidance Digital Signal Processor including logic synthesis, timing closure, floorplanning and physical design, DFT, scan and JTAG insertion, and ATPG
- Independent design review and risk analysis of mixed signal ASIC prior to prototyping

Kaiser Electronics, San Jose, CA
- Behavioral modeling and simulation of system components for aircraft display processor. Simulation, static timing analysis, test vector generation for DMA Controller ASIC. Logic design for Frame Buffer Controller ASIC. Image processing algorithm development using C.

EMPLOYMENT HISTORY – 1982 to 1989

Seattle Silicon, San Jose, CA - Sr. Applications Engineer
- Design support for design rule based silicon compilation software. Pre- and post-sales support including demos, benchmarks, die size estimates, presentations and customer training.

Array Technology, San Jose, CA - Sr. Design Engineer
- Logic design, verification, layout and test of ASICs, SPICE circuit analysis, design rule checks. Lab work characterizing CMOS ESD protection of SCSI IO cell, analyzing results and redesigning cell. Designed nonvolatile real-time clock device including battery backup and charging circuitry.

Citel, Inc., Santa Clara, CA - Design Engineer
- Logic design, verification, layout and test of ASIC products, SPICE circuit analysis. Full custom circuit design and layout, cell library development, process design rule development and checking.

American Microsystems, Santa Clara, CA - Design Engineer
- Logic design, verification, layout and test of ASIC products. SPICE circuit analysis, design rule checks, lab work for failure analysis.

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SPECIALIZED SKILLS

Synopsys Design and DFT tools, Primetime, VCS, Modelsim (Questa), NCVerilog, Verilog HDL, VHDL, AVANT! Jupiter and Apollo, Mentor Graphics DFT and layout, SPICE, C, C++, shell scripting, Perl, Tcl

PUBLICATIONS

- "Synthesis of a 200K Gate Array", Synopsys User's Group Meeting, March, 1995
- "Comparing Two Verilog Fault Simulators", Integrated System Design, October, 1995

EDUCATION

Bachelor of Science - Electrical Engineering ◆ University of the Pacific ◆ Stockton, CA (1982)

PROFESSIONAL AFFILIATION

Professional And Technical Consultants Association (PATCA) since 1993
Cadence Verification Alliance since 2006